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Application Serial No. 10/617,754

Response to Official Action dated 25 May 2005

REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the Official Action dated 25 May 2005. Responsive to the rejections made by the Examiner, Claims 1, 10, 11, 14 and 15 have been amended and are now clearer in their respective recitations. Claims 2 – 7 have been cancelled by this Amendment. Claims 1 and 8 – 17 will be pending in this Application upon entry of this Amendment.

In the Official Action, the Examiner rejected Claims 1 – 17 under 35 U.S.C. § 102(b) as being anticipated by Gulick, et al. (U.S. Patent # 6,148, 357; hereinafter Gulick). In setting forth the rejections, the Examiner observed that Gulick discloses a link bus using an arbiter for controlling bus directional modes.

Applicant's invention overcomes shortcomings of the prior art by avoiding delays in bus access attributable to various arbitration schemes. As the amended claims now more clearly recite, "a request signal [is transmitted] only over a first request signal line from said second control chip to said first control chip to request control of said first AD bus by said second control chip". Subsequently, "address and data [are transmitted] from said first control chip to said second control chip through said second AD bus only if said second control chip is not transmitting on said second AD bus at a time of receipt of said request signal". Thus, the transmission of arbitration data over the bus is avoided, thereby avoiding the decrease in bandwidth due to the arbitration data traversing the bus and,

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additionally, avoiding the waiting periods associated with the arbitration procedure before access to the bus is granted.

The full combination of these and other features of Applicant's invention are nowhere disclosed by Gulick. Whereas, Gulick has certain features in common with the invention of the subject Patent Application, the bus access procedure disclosed by the reference relies upon the arbiter 509 to determine the appropriateness of the transition into the whole-bus mode and arbiter 507 for determining which requester will be granted access to a half-bus. As clearly shown in Fig. 7, Gulick passes arbitration requests on the bus in both half-bus and whole-bus modes, thereby presenting a significant decrease in bandwidth. Such mechanism is clearly removed from "transmitting a request signal only over a first request signal line from said second control chip to said first control chip to request control of said first AD bus by said second control chip", which is neither shown nor suggested by the reference. Thus, as Gulick fails to disclose each and every element or method step of the subject Patent Application, as now claimed, it is respectfully submitted that the reference cannot anticipate the invention so claimed.

Furthermore, the arbitration disclosed by Gulick involves the passing of request and acknowledgement messages to accommodate various timing and bus access modes, as described in the reference. Applicant's invention involves no such complexity in "transmitting addresses and data from said first control chip to

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said second control chip through said second AD bus only if said second control chip is not transmitting on said second AD bus at a time of receipt of said request signal", thereby avoiding delays associated with the bus arbitration of Gulick and other techniques of the prior art. Moreover, Gulick, to implement the extensive arbitration requirements, installs an arbiter on both the link and protocol layers, which is avoided by Applicant's invention. Thus, as Gulick teaches away from Applicant's minimal arbitration for the objectives stated in the subject Patent Application, it is submitted, respectfully, that the invention thereof, as now claimed, is not made obvious by Gulick.

Independent Claim 1 recites where "said first [and second] control chip undergoes a transition from said first [and second] unidirectional mode to said first [and second] bidirectional mode only upon said second [and first] control chip receiving said first request signal while not transmitting on said second [and first] address/data bus", which is not shown or suggested by Gulick. Thus it is believed that Independent Claim 1, as now amended, is allowable. Independent Claims 10 and 14 recite the limitations of "transmitting a request signal only over a first request signal line from said second control chip to said first control chip to request control of said first AD bus by said second control chip" and "transmit[ting] addresses and data from said second control chip to said first control chip if said first control chip is not controlling [or transmitting on] said first AD bus at a time of receipt of said request signal", which is also neither

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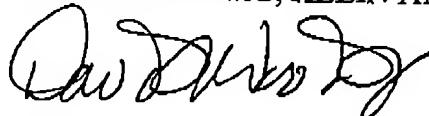
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disclosed nor suggested by Gulick. Thus, Independent Claims 10 and 14 are also believed to be allowable. Additionally, the Dependent Claims depending from Claims 1, 10 and 14 are believed to be allowable for at least the same reasons for which their corresponding base Claims are allowable.

The remaining references cited by the Examiner but not used in the rejections have been reviewed, but are believed to be further remote from the subject Patent Application than the reference used by the Examiner when patentable considerations are taken into account.

It is believed that the subject Patent Application is now in condition for allowance and such action is respectfully requested.

Respectfully submitted,  
For: ROSENBERG, KLEIN AND LEE



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Dated: 26 SEPTEMBER 2005

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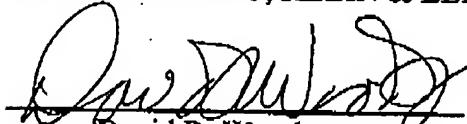
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I hereby certify that this paper is being facsimile transmitted to the U.S. Patent and Trademark Office, Art Unit # 2111, at (571) 273-8300, on the date shown below.

For: ROSENBERG, KLEIN &amp; LEE



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26 SEP 2005

Date

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